**Latches:**

Nor=active high ;nand=active low. Reset e Q jetai thakuk output=0. set e Q jetai thakuk output=1

Active high : .0-0=no cheng, 0-1=reset;1-0=set; 1-1=invalid Active low : 0-0 =invalid, 0-1=set.;1-0=reset; 1-1=no change.

S-R latches : extra input enable(more control), enable=0=no change; enable=1=same as active high;

D latches:enable =0=no-change; enable=1 (1) D=0 Hole Q=O; (2)= D=1 Hole Q=1; INVALID OR NO CHANGE STATE NAI. **Inverter add kore sr-latch D latch e neya jay**

**Flip-Flops**

rising edge=positive; falling edge=negitive; D Flip-Flops= clock pulse= D = HIGH=SET=Q = 1, Q’ = 0

D Flip-Flops= clock pulse= D = low=RESET=Q = 0, Q’ = 1,prallel data stor

JK flip-flops=no invalid state.1-1=toggle.baki sob active high latches

**SR= both input are high**

**Sr flip flop to d flip flo= single not gate add;**

Application of Flip-Flops: N flip-flops frequency by 2^N. Each flip-flop frequency =2

**N flip-flops are required for N-bit counters.**

benefit =frequency division duty cycle is exactly 50%.

**Latch = 1.kono clock single nai 2.level sensetive.**

**Flip flop=1. clock single 2.edgs sensetive**

**Counters**

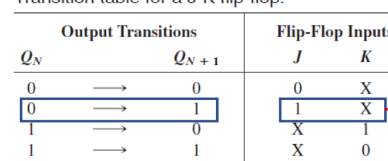
Asynchronous Counter=flip-flops do not have a common clock, do not change states at the same time.

Synchronous Counters :the flip-flops have a common clock, flip-flop changes its states at the same time.

**MOD Counters**

N bit =2^N counting state;MOD-N=N-bit counting state.

MOD -10=counting state =10,max-count=9(10 state); reset =11th state; **flif flop=max-count er binnery form**

**Irregular Sequence Counter**

**555 Timer(2 ta comprator,3 ta resistor,2 lathes)**

Trigger= Kono kisu suru kore deya. Thresold= konokisur limit ke bujay.

**COMPARATORS:**

Uper comprator =high=reset;; lower comprator =high=set;;

Thresold voltage>=control voltage=1; Thresold voltage<control voltage=0;

Latch=set=switch of=discharge path =discounected;; Latch=reset=switch on=discharge-path=counected;;

**Modes of Operation**

Astable Mode= Two resistors ,One capacitor;; Monostable Mode= One resistors,One capacitor The width of the pulse is : TW = 1.1R1C1 ,

Astable Mode :TH = 0.693C1( R1 + R2), TL = 0.693C1(R2), T = TH + TL = 0.693C1(R1 + 2R2),

F = 1 /0.693C1(R1 + 2R2), D. C. = TH/ TH + TL

**Quantization**

**N-bit ADC ;;**2^N=Resistor,(2^N)-1=comprator,,one 2^N to N priority Counter.

**RAM(**Random Access Memory)

both read and write capability., volatile,

**ROM(**Read Only Memory)

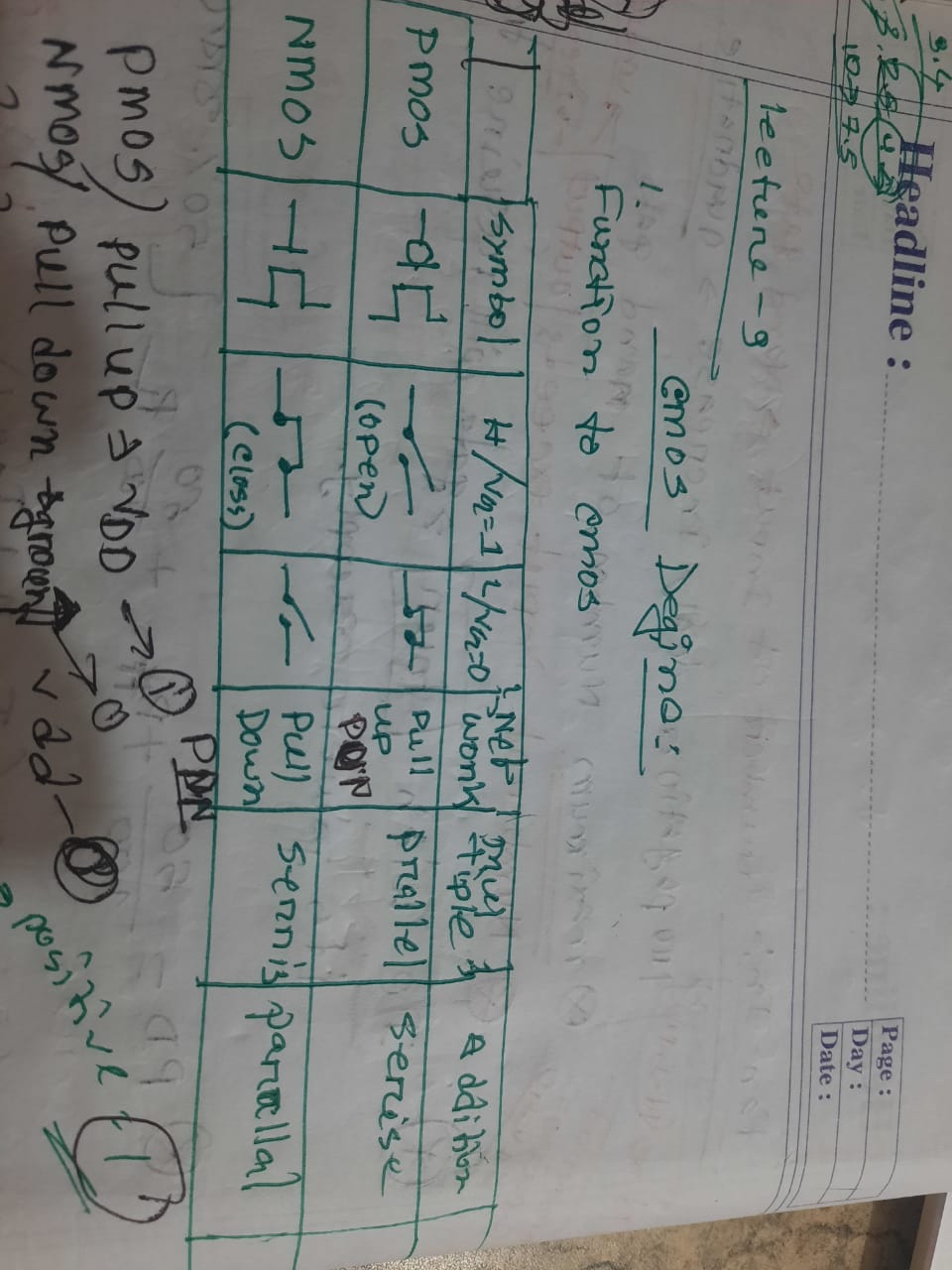
Read, no write, nonvolatile

SRAM DRAM:

1.uses Latches as storage elements 1.uses capacitors as storage elements.

2.SRAMs are faster. 2.DRAMs are slower.

**CMOS**

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UPORE VDD ER SATHE PULL Up network.